FACULTY PROFILE



**RAMESH BABU CHANDIKA**

Department: Electronics and Communication Engineering College: Seshadri Rao Gudlavalleru Engineering College Mobile: 9494475775

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**Address for Communication:**

**College Address:**

Ramesh Babu Chandika

Assistant Professor,

ECE Department,

Seshadri Rao Gudlavalleru Engineering College,

Andhra Pradesh: 521356

**Academic Qualifications:**

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| --- | --- | --- | --- | --- | --- |
| **S. No** | **Name of the Degree** | **University** | **Percentage of Marks/Grade** | **Specialization** | **Year of Pass** |
| 1 | M. Tech | JNTUKUniversity | 84.25% | VLSI System Design. | 2016 |
| 2 | B.Tech | JNTUKUniversity | 68.61% | ECE | 2012 |
| 3 | Diplamo | SBTET | 69.58% | ECE | 2009 |
| 4 | Intermediate | Board of Intermediate Education | 84.20% | MPC | 2007 |
| 5 | SSC | Board Of Secondary Education AP | 60.83% | - | 2005 |

**Teaching Experience: 2.6 Years.**

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| --- | --- | --- | --- |
| **S. No.** | **Designation** | **Institution Name** | **Working Period** |
| **From** | **To** |
| **1** | Assistant Professor | Seshadrirao Gudlavalleru Engineering College | 30-07-2025 | Till date |
| **2** | Assistant Professor | Dhanekula Institute of Engineering & Technology | 01-07-2023 | 28-07-2025 |
| **3** | Assistant Professor | Sasi Institute of Engineering & Technology | 18-01-2023 | 18-05-2023 |

**Professional Body Membership**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Name of the Professional body** | **Membership Number** |
| **1** | International Association of Engineers (IAENG) | 515314 |

**PROFESSIONAL SKILLS:** ¬ Strong knowledge of Verilog HDL, System Verilog, C/C++, Mentor Graphics- Questa sim, RTL Coding using Synthesizable constructs of Verilog.

**Papers Published in Journals No. : 02**

1. Ch. Ramesh Babu, K.Saisudheer **“*Low Power & Area optimized FPGA Design with Autonomous Power Gating and LEDR Encoding***” International Journal of VLSI Design and Communication Systems Volume No.3, Issus No.10, December 2015.
2. Ch. Ramesh Babu, “**Advanced SPI Controller with Enhanced Features For VLSI Integration” J**ournal of **N**onlinear **A**nalysis and **O**ptimization Vol. 15, Issue. 1: 2024 ISSN: **1906-9685**

**Subjects Handled:**

**Theory:**

1. Basic Electrical and Electronics Engineering

2. Electronic Devices and Circuits.

3. Microprocessors and Controllers

**Labs:**

1. Electrical and Electronics Workshop (EEWS)

2. VLSI Lab.

3. IoT & ARM Lab.

**NPTEL Certification Courses:01**

1. DIGITAL CIRCUIT DESIGN – 52%

**Training Programs /FDPs/Workshops Attended No: 15**

1. Attended a Two-day workshop on “ARM and Microprocessor design and programming “at GEC, Gudlavalleru on September 7th&8th2015.

2. Attended a one day workshop on “Maintenances of Electronics Lab Equipment “at GEC, Gudavalleru in February 29th 2016.

3. Two day training program on " Simulation of Linear & Digital Integrated Circuits and Microcontroller based Applications" using NI Multisim organized by the Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru on 4-5 November 2016.

4. Attended a Two day workshop on "Mentor Graphics Tools" at GEC, Gudlavalleru in August 31th & 1st September 2017.

5. Organized a Twoday workshop on "IoT Platforms and Their Practical Implementation" at GEC, Gudlavalleru on December 8th& 9th 2017.

6. Attended a One day workshop on “High-Frequency Structure simulator (HSFF) “at GEC, Gudavalleru in February 29Th to 30th 2019.

7. Attended a Two day workshop on “Design and Development of VLSI Circuits using Mentor Graphics Tools “at SRGEC, Gudavalleru in December 14Th to1 5th 2020.

8. Attended a Two days Faculty Training program “Full custom design using CADENCE “at SRGEC, Gudavalleru in August 4Th to 5th 2022.

9. Attended a Two days FDP on “Network Simulation with Net Sim Software “at SRGEC, Gudavalleru on August 13Th to 14th 2022.

10. Attended an AICTE Recognized Faculty Development Program on” Antenna Design Techniques and Tools” at Dhanekula Institute of Engineering and Technology, Vijayawada, Andhra Pradesh from 11/09/2023 to 15/09/2023.

11. Attended a Three days FDP on “Engineering Trends in VLSI Device, Circuit System Design-A Practical Approach “ at R.V.R & J.C College of Engineering in November 09Th to 11th 2023.

12. Attended an AICTE Training & Learning (ATAL) Academy Faculty Development Program on “Design Thinking and Prototyping for Industry 4.0 “at SHRI VISHNU ENGINEERING COLLEGE FOR WOMEN from 20th November to 25th November 2023.

13. Attended a one-week Faculty Development Program on "**Emerging Trends in Embedded Systems and 6G Communications**" organized by the Department of EECE, GITAM School of Technology, GITAM Deemed to be University, Visakhapatnam, during 12th- 16th May 2025.

14. Attended a one-week Faculty Development Program “**Recent Trends and Innovations in Advanced Computing and Intelligent Systems"**. Organized by the School of Computer Science and Engineering, VIT-AP. *University, Amaravati from 2nd to 6th June 2025.*

**Declaration**

I hereby declare that all the above-furnished information is correct to the best of my knowledge.

Date: Signature

Place: Gudlavalleru (Ch. Ramesh Babu)